Amimul Ihsan

Email**:** amimul_ihsan@yahoo.com
Phone: (802) 829-2826. **Website**: muehsan.com

Summary:

- Multiple years of Hands-on experience covering RFIC Design, RF System Design, Characterization on RF modules in Lab for Gain, Linearity. Digital Circuit Design and Layout with advanced EDA tools. Design for optimum area, power, and speed. Design for Robustness; EM, IR drop and Noise.

- **Designed LNA, Power Amplifier, VCO,** Shifter and Mixer. Matching Network. **RF System Test.**
- Designed and **tested most of the components of Receiver Chain and Sensor.**
- Experience in a variety of RF frequency bands. Microwave Design in GHz frequencies.
- RF Link Budget analysis using ADS for Gain, Noise, Harmonics, Nonlinearity aspects such as IP3, P1dB.
- **RF Lab:** Using Vector Network Analyzer (VNA), Spectrum Analyzer (SA), Signal Generator (SG), DMM.
- Tested HPA, PA, LNA, Syx, Up/Down Convert, Filters. S21, S11, S22. Bands: VHF, UHF, VLF, L & K Bands.
- RF SSPA for Linearity, **Harmonics**, Gain, Power, Heating. PA Classes.
- **Familiar with:** Transceiver Chain, EMC, EMI, Antenna design, SDR and e'-W.

- **Electronic Design:** *Designed high speed memory and other circuits for leading edge microprocessors.*
- Experience with several generations of Technology; 7nm-180nm CMOS. GF-45nm, SiGe, SOI & GaN.
- Experience with post-silicon HW debugging and failure analysis and diagnosis of digital circuits.
- Experience with microelectronics in extreme environments (high/low temperature and etc.).
- Extensively used Advanced EDA tools (**Virtuoso**, Synopsys, etc.): ***HSPICE.*** **DRC/LVS/**EM/NOISE/IR drop.
- Familiar with: Cryogenics, Quantum Entanglement, Annealing, JJ, SQUID, Superconducting Circuits.

- **Leadership and Communication skills:**
  A) Trained and guided RF and Electronic Engineers in high tech.
  B) Experience with the initial concept to successful product. Led team in the RF Lab.
  C) Presented developments and reviews to Internal and External technical audience.

- **Stanford University, CA. MS. Electrical Engineering.**

Consulting Engineer: 2023-Present.
RF Design/Test Engineer: Worked on projects for Boeing and other corporations.
- Design Overview of Solid-State Power Amplifier (SSPA) and Multiport Transceiver Systems for SLS.
- Helped with techniques to mitigate issues on: Linearity, Gain, Power Consumption.

Northrop Grumman Mission and Missile System: 05/2020-2022
Lead RF System Staff Engineer:
- Matching LNAs and PAs using VNA, SA, SG for Gain and optimizing S parameters for Transceivers.
- Conducted research to acquire the best Wireless Access Point and RF-Coupler. P1dB and IP3.
- Contributed on ICA (Intra Flight Data Link Control Module), Top level and Sub-Assembly MRE.
- Tested multiple PA (Power Amplifier), Synthesizers and Up-Down Converters) with Functionalities.
- Built and tested MADL (Multifunction Advanced Data Link) Electronics. LabVIEW programming.
- Worked on Telemetry and RF Communication Architecture for Optical Network.
- Proposed secondary and tertiary communication for DWDM**.** Some Agile/Scrum and JIRA.

Lockheed Martin Space Company. Sr. Staff RF Engineer: 12/2018-02/2020
- **RFIC Design**: LNA, PA and Mixer. Used extensively Cadence RF-Spectre Simulator. Simulated *Nonlinearity aspects such as IP3, P1dB.* Worked on Integrated Circuit Design. Wrote MATLAB codes for GPS III Satellite.

- Heterogeneous Package: RF Link Budget Analysis on Gain, Non-Linear, Noise, Harmonics; with ADS.
- Contributed to the GaN process developed at Lockheed.
- **Filed invention disclosure**: **1)** Fixing LNA Gain Loss on board **2)** Enhanced Power Amplifier.

IBM Microprocessor Design Team. Senior Design Engineer: 2018 and 2004-2006

- Worked with silicon debugging team on the level 1 caches diagnosing circuit and timing related hardware issues. Held design reviews on I and D-Caches. Functional Verification using ESP-CV, Verity, VGEN. Worked on the RISK Microprocessor for the Nintendo Wii chip that was widely successful.
- Designed and implemented in engineering UNIX/LINUX workstations, Cadence's Virtuoso tool and IBM's internal tools such as Power Spice, Erie extraction, Niagra DRC, LVS, TLT and functional verification tool Verity. SOI integrated circuits containing complex Digital circuits. Static timing analyzer tool to analyze setup/hold time violations. Optimized WL of I and D Cache.
- **ASIC Design**: Analyzed Analog and Memory circuit (Cadence-Spectre) with 7nm Technology. Interpreted data, analyze results using Monte Carlo Simulation (statistical techniques).

RFIC Design: Designed SRAM, LNA, PA and Voltage Controlled Oscillator. 2011-2017

- **Teaching Assistant**: *Graduate Courses. Electronic and Optical of Device and Lasers in Material Processing.*
- **Research Assistant**: *Conducted research on how to make very low power devices for next generation devices beyond* Tri Gate and FinFET**.**
- Designed Low Power and High Efficient Voltage Controlled Oscillator, VCO.

Sun Microsystems (Oracle). Member of Technical Staff: 1998-2000 and 2006-2009

- Designed 64-bit dynamic shifter. Simulated the I-cache for Microprocessors.
- Designed high speed Carry Look Ahead Static Adder for floating point unit**.** Wrote Verilog for Adder.
- **Modelled and Evaluated** speed, functionality, feasibility of 64-bit dynamic shifter using HSPICE and state of the art **CMOS technology**. Characterized Power, Area, Noise**,** EM and IR drop on large digital circuits.
- Verification Flow: Innologic, Verplex. STA, ATPG, Clock: NCVF, Sigem, **Noise**, SERF.

AMD & ARM. Microprocessors Digital and Memory Circuit Design:

- Designed SRAM's core cell and its peripheral circuitries using CMOS technology. Optimized designs to meet required memory access time. **Trained Junior engineers on Design Tools and Verification Jobs.**
- Designed different Memory and Datapath modules for Leading Edge Microprocessors.
- Completed Bit cell simulations to determine the ratio of Read to Leakage current. Programmed EEPROM.

Education:

MSEE. Stanford University, Stanford, CA. 2013

Graduate Courses: RF Integrated Circuit Design, Advanced Analog IC**,** Advanced Digital IC Design and Advanced Semiconductor Device, Computer Architecture and Optical Micro-Nano Cavities.

BS Electrical Engineering: Texas, USA (Scholarship and State Public Grants).

Software Skills, SW operating systems, Packages:

UNIX, LINUX, MS Windows/NT, OFFICE, MS PowerPoint, MAC OS, SOLARIS and Visual Studio

- C#/C++, Java, Python, Assembly, UNIX shell, MATLAB and LabVIEW programming.

Tools: Keysight**:** ADS**. Cadence**: Virtuoso, RF-Spectre, OrCAD**,** Schematics/Layout, Verilog and DRC/LVS/ERC. **Synopsys**: HSPICE, PathMill, Starsim, StarRC & ESPCV. **Mentor Graphics** DA & EDA tools. IBM Tools**:** Powerspice, GYM, SpiceJoules, DOORS, APDP and HFSS.